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1 I Pages 19-21 describe preferred generic concepts of a 3D array. Claims 99-120 and 456-481 are directed to this feature. Fig. 35-36

2 II Pages 22-49 describe the pillar device embodiment. Claims 1-12 are directed to this feature.

3 III Pages 23-43 are directed to pillar TFT EEPROMs, while pages 48-49 are directed to the diodes. Claims and 64-98 and 13-63, respectively, are directed to these features. 35 9 diodes.

4 IV Pages 49-73 are directed to self aligned TFTs. Claims 121-217 are directed to these features.

5 V Pages 74-86 are directed to rail stack TFTs. Claims 218-337 are directed to these features. Fig 52.

6 VI Pages 86-97 are directed to a flash rail stack TFT memory. Claims 401-448 are directed to these features. Fig 68-82

7 VII Pages 97-106 are directed to a CMOS logic array. Claims 338-400 are directed to these features. 83-86 87-92

8 VIII Pages 106-111 are directed to metal induced crystallization in a TFT. Claims 449-455 are directed to these features. Fig 93-96

Generic Ideas	Drivers in Substrate C-99 ⟺ Fig. 35
456, 467, 475 3D - with CMP	C-106-120 ⟺ Self aligned

456-482